Technical Handbook

SE 550-08-25-1

Part 3

Functional Description

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3 FUNCTIONAL DESCRIPTION

3.1 General

The Mobile transceiver SE 550-08-25-1 is controlled by two processors. One processor is in the transceiver and the other is in the control unit BG3.

Transmit and receive frequencies are generated with two independent synthesizers. The operating software is stored in an EPROM. Specific parameters depending on the carrier network are stored in a RAM and can be modified by way of the data or the coding plug.

3.2 Rx Branch

3.2.1 Rx Signal Path

(1) Signal Path in the RF Stage

See circuit diagram: receiver 0850.210.210.201A

The PLL receiver operates with a synthesizer of its own in accordance with the double super principle. The antenna signal arriving from the antenna socket passes through the antenna low pass (0832.300) and is passed through a three-pole plug connector to the RF stage (0850.210).

During transmission, + 9 V level is applied via L1. D1 becomes conductive and shorts the RX input.

No DC voltage is applied during reception. D1 is reverse biased and the signal path via L1 and C2 to the filter L2 is open.

The Rx signal is passed through the dual circuit band filter L2 (preselection), the first buffer amplifier stage V1 and the triple circuit band filter L6 (main selection) to the FET mixer V2.

After band selection and signal amplification (V1), the signal is converted to the first intermediate frequency (IF1) of 21.4 MHz with the FET mixer V2. The signal of the Rx oscillator is monitored and regulated by the synthesizer module and is frequency stabilized to a high precision. It is forwarded to the FET mixer V2 via LB.

The differential signal from the carrier and Rx oscillator frequency (Ist IF) passes through the quartz crystal filter Q1. The frequency response of the quartz crystal filter Q1 is influenced with L12 and L16 (wobbulation curve).

Via the IF stage V4, the IF signal is amplified and forwarded to the discriminator in the IF component J1.

The diodes D16 and D17 serve to limit the input signal for the IF component J1. The IF component J1 contains the second IF oscillator (with Q3 = 20.945 MHz or Q2 = 21.855 MHz), the second IF stage (with QF = 455 kHz ceramic filter) and the demodulator (phase shifter circuit L21, C63, R40).

The unfiltered AF signal is passed from the output of the discriminator (J1/9) via the high pass filter J7.II to the squelch submodule (0831.250) and via the AF low pass filter J7.I to the low pass Rx submodule (0831.290).

The squelch signal RSP is forwarded via the connectors B3/9 --> B3/3, and the AF is forwarded via connectors B3/8 --> B3/2, to the control assembly (0950.410).

(2) Signal Path in the Control Assembly

Refer to the trunking control circuit diagram 0850.410.210.003

On the control assembly (0850.0410), the prefiltered AF signal is picked up at B3/2 and is fed via a switchable analog active filter chain. Data signals at tapped at J2/1 and are made available to the FFSK evaluator on the MPT 1327 modem (0831.470).

The AF path can be deactivated at the analog switch J3/1. By way of J3/2 it is possible to feed signals into the receiver or loudspeaker when the receive path is deactivated.

J3/3 renders the demodulation characteristic switchable according to the deemphasis characteristic.

The signal is forwarded via B6/4 to the AF amplifier on the stabilizer board (0831.140) and is passed via the interconnection board (0831.110) to the unit's loudspeaker. With J26 on the control board the loudness level is determined.

3.2.2 Receiver Phase Control Loop

See circuit diagrams:

Receiver	0850.210.210.201A
RF control	0850.210.310.201B
VCR receiver	0832.510.410.002

The SE 550-08-25-1 has as its reference oscillator (TCX0 0833.560) a temperature-compensated crystal oscillator containing crystals of maximum quality. The TCXO generates the reference frequency. This is forwarded to Pin 1 of the synthesizer J3, which forms a PLL stage together with VCO RX, the buffer stage V8 and the frequency divider J2.

The synthesizer J3 receives the frequency information serially via J3/10, which is forwarded to J2/6 according to the predivider ratio. An analog setting voltage, which sets the frequency-defining phase circuit of the VCO RX to the corresponding frequency range, is generated by way of the digital/analog converter J4 (RF control assembly circuit diagram) and is forwarded via the OP amplifier J14 to the VCO RX (VCO Rx circuit diagram) and to the capacitance diodes D3, D5, D8 ... D15 and D45 (receiver circuit diagram) for selection tuning.

The VCO Rx supplies a precise local oscillator frequency. It is forwarded through the buffer stage V8, divided by 64/65 in the predivider J2 and is passed on to the main divider in the synthesizer J3. Here, in the phase comparitor it is compared against the reference frequency applied to J3/1 and supplied by the reference oscillator TCXO, which is also divided. In the event of a deviation from the TCXO frequency, an analog control frequency is generated that cancels the frequency deviation.

The processor on the control board (0850.410) supplies the digital necessary for the main divider in J3. The phase comparitor therefore generates a control voltage proportional to the phase deviation that readjusts the VCO Rx (MP 2).

3.2.3 VCO for the Receiver

Refer to the circuit diagram of the VCO Rx 0832.510.410.002

The function of the oscillator V1 is defined by the capacitive voltage divider C7 and C8. The setting voltage fed to P2 modifies the capacitance of D2...D4, thus modifying the phase condition. The generated frequency is coupled via the buffer stage V2.

The control at P3 generated with the PLL circuit modifies the capacitance of D5. This counteracts a frequency deviation.

3.2.4 Low Pass Rx

Refer to the low pass Rx circuit diagram 0831.290.410.001

The low pass Rx lends a specific frequency response characteristic to the AF in the demodulation path. The AF signal is fed to the impedance converter J1/II via the low pass filter R1/C1, R3/C2, J1/I and RC low pass filter R2/C3.

The Rx low pass board is soldered onto the RF stage board.

3.2.5 Squelch 12.5 kHz

Refer to the squelch 12.5 kHz circuit diagram 0831.250.410.101

The AF signal is applied via a band pass filter and the impedance isolation stage V1 to the filter chain containing D1 and D2 for rectification. At the output 7, the hysteresis amplifier J1/II switches the RSP criterion between high and low level. The hysteresis is defined by negative feedback with R11 and R12 (test shop value).

The squelch board is soldered onto the RF stage board as a subboard.

3.3 Tx Branch

3.3.1 Tx Signal Path

Refer to the trunking control circuit diagram 0850.410.210.003

Modulated analog voice signals, which are fed to the VOC TX (0832.510) via the modulation path (analog input filter chain) are sent, or data signals that are fed into the active AF filter path.

The microphone signal at B5/1 of the display board (0831.920) in the control unit is applied to B1/14 of the control board. The nominal deviation of the modulated carrier is set with the potentiometer R65. By means of software, the preemphasis characteristic can be switched over on the analog switch J23/1. The microphone or data signal is selected with J23/2. DTMF data (optional board) or FFSK data (MPT 1327 modem 0831.470) can be routed into the modulation path.

The respective signal is amplified in linear fashion with J22/2. The deviation is set with the potentiometer R111.

The operational amplifier chain and the analog switches receive idle operating potential U/2 from the impedance converter J25/2. Thus, the deviation symmetry can be influenced via the potentiometer R96.

3.3.2 Transmitter

See circuit diagrams:

Transmitter	0850.210.310.210C
RF control	0850.210.310.201B

Via the low pass Tx submodule (0831.280), the modulation signal is forwarded to the max. deviation regulator R150. It is then fed into the VCO for the transmitter (VCO TX 0832.510) for direct VCO modulation. Together with the synthesizer J12 and the predivider J11, the VCO TX constitutes a PLL stage which operates like the Rx oscillator PLL stage.

As in the case of the receiver, a setting voltage for coarse tuning of the VCO TX is generated by the digital/analog converter J13 and the amplifier J14 (circuit diagram: RF control). This is adjusted with R150.

V30 (circuit diagram: transmitter) serves to switch over the phase locked loop for swift latching or slow settling within the scope of modulation. The phased or non phased state of the PLL stage is interrogated via J12/7 (unlock Tx).

The modulated carrier is routed via the amplifiers V18, V19, V20 to the Tx module J16, where maximum power amplification is realised.

Power regulation for the Tx module J16 is realised by way of the differential amplifier V26 and V27. The current level of the differential stage is adjusted with R117 (power adjustment).

By means of software, the Tx power can be switched in a maximum of three stages at the base of V26 (see RF control J15, pins 11, 12).

3.3.3 VCO for Transmitter

See circuit diagram of VCO Tx 0832.510.410.502

The frequency of the oscillator V1 is defined by the capacitive voltage divider C7 and C8. The setting voltage fed to P2 alters the capacitance of D2...D4 and therefore alters the phase condition. The generated frequency is coupled out via the buffer stage V2.

The AGC voltage at P3 generated with the PLL circuit alters the capacitance of D5. This counteracts a frequency deviation.

The modulation signal for VCO modulation is fed via P1.

3.3.4 Low Pass Tx

See circuit diagram: low pass Tx 0831.280.410.002

The low pass Tx lends a specific frequency response characteristic to the AF in the modulation path.

The AF signal is fed via the input amplifier J2/II the and active low pass chain of the fourth order, which consists of the OP amplifiers J2/I and J1/1.

The low pass Tx board is soldered as a subboard onto the RF stage board.

3.4 Reference Oscillator TCXO

See circuit diagram TCXO 0833.560.410.001

The temperature-compensated reference oscillator is soldered onto the RF stage board as an independent shielded submodule.

The binary counter in the counter component J1 generates an exact 400 kHz signal from the 6.4 MHz reference signal of the oscillator V1. This is made available to the synthesizers of the two PLL stages in the Rx and Tx paths.

The board also contains a voltage cascade to generate a 24 V DC voltage. This produces an extended setting voltage range for the VCOs or for input selection.

3.5 Antenna Low Pass

See circuit diagram: antenna low pass 0832.300.410.002

On reception, the carrier signal arriving from the antenna socket passes through the passive LC low pass filter and is made externally available at B2.

The signal path is reversed in the transmit mode. Harmonics are cut off by the LC filter chain.

The antenna low pass is accommodated in a shielded housing.

3.6 Interconnection Board 25 W

See circuit diagram: interconnection board 0831.110.410.001

The 15-pole central connector B1 and the five-pole data connector B2 for cloning are attached on the interconnection board.

Signal separation to the control and RF stage boards takes place on the interconnection board.

The $+U_B$ line is fused with the fuse link F1.

3.6.1 Cloning

Via the connector B2, which is accessible on the rear panel, data, including cloning data, can be exchanged with an external data transceiver. The external data transceiver is then a PC with which interactive parameter programming (IPP) is realised, or with which a different Se 550 is cloned.

3.7 Control

See circuit diagram: trunking control 0850.410.210.003

3.7.1 Processor with Memory

The microprocessor J11 is clocked by an 11.0592 MHz crystal. It works together with the ASIC J12 for the addresses and with the memory components J13 (EPROM) and J14 (RAM) for process data transfer. The ASCI 12 generates frequency signals with defined timing conditions for different signalisation tasks.

3.7.2 Process Periphery

The operating voltage of the processor is monitored and the defined power on reset is generated with J7. The EEPROM J8, through which data can be output serially, offers an additional memory option.

The enable signals of the shift registers (type 4094) are controlled in the unit with J10 as a 1 out of 10 decoder.

J17 and J18 are further interfaces for data poling. The data is applied in parallel to the respective component and is poled serially. Status information and system data are acquired in this way (ON functions, RSP etc.). The components J9, J5 and J6 are serial input, parallel output shift registers for process data transfer.

The volume of the AF can be set in five levels. This is done with the analog multiplexer J26 and the shift register J6.

3.7.3 MPT 1327 Modem

See circuit diagram: MPT 1327 modem 0831.470.410.001

With its 1200 baud FFSK modem J1, the MPT 1327 modem (0831.470) enables processing of the special data format confirming to MPT 1327 for trunking operation.

The level of the two sinusoidal FFSK key frequencies (1200/1800 Hz) is set to 0 DBM with R2.

3.7.4 Tone Signalisation

Tone signalisation is realised by the tone multiplexer J20/2. From here, the generated signals can be passed through J20/3 and the amplifier J25/1 into the modulation path (transmitter) or into the AF branch (receiver path).

3.7.5 Operating Data Backup (option)

As an option, a lithium battery can be installed on the stabilizer board (0831.140). The lithium battery applies a back up voltage to J14 (RAM) via B2/4. This ensures that the current operating information remains stored even when the unit is removed.

3.7.6 Temperature Monitoring

In the event of inadmissible overheating, the unit is switched off with V8 and the PTC resistor R55.

3.7.7 Center Voltage

The center voltage (+U/2) required for functioning of the filter chains is derived from +9 V with the voltage divider R94, R95, R96. It is available at the output of the impedance converter J25/2. The deviation symmetry is set with R96.

3.8 Stabilizer Board

See circuit diagram: stabilizer board 3 W 0831.140.310.002

+9.3 V stabilisation

On the board, a stabilized voltage of +9.3 V is derived from the operating voltage +UB and is made available at B3/6. The stabilisation circuit is switched on/off with ON signal at B6/2.

+5 V generation

A voltage of +5 V is generated with J3 from the +9.3 V voltage and is used to power the digital ICs via B6/1.

Loudspeaker amplifier

The AF for the loudspeaker is fed to B6/4 and is amplified with J1.

Controlled by the processor, the loudspeaker can be switched on/off via the input B6/3. When the loudspeaker is ON, +UB is switched to the AF amplifier J1 via V3 and the Darlington stage V1, V2.

Lithium battery (option)

As an option, a lithium battery can be installed on the stabilizer board.

The lithium battery generates a voltage for powering the RAMs J14 on the control board (0850.410). This guarantees that the operating data stored in the RAM will not be destroyed in the event of a power failure or removal of the unit.

3.9 Control Unit BG 3

3.9.1 General

The control unit is available with different operating interfaces (key pad) depending on the application.

Unit and user system information is visualised on the two-line vacuum fluorescent display and on the status symbol displays.

The control unit is controlled by a microprocessor on the display board.

3.9.2 Key Board

See circuit diagram: key board 0831.930.310.001

The statuses of the coded keys are interrogated by the microprocessor of the display board via the connector B2. The microprocessor sends serial display data via B1 and the shift registers J1 and J2. The LEDs D27...D42 for illumination of the symbols are controlled via the outputs of the shift registers.

The footer transistor V2 measures the ambient luminous density and controls the brightness of the display unit.

Switched by V1, the LEDs D1...D26 illuminate the key pad on the control unit.

The "On" key T26 serves to switch the unit on/off.

3.9.3 Display Board

See circuit diagram: display board 0831.910.110.005

The connectors B1 and B2 connect the display board to the key board, B4 to the coding plug, B5 to the microphone and B3 to the converter board.

A microphone amplifier (J101/I) is connected between B5/1 and B3/18 and can be rendered inactive by jumpers (Br9) whenever the microphone level requires no further AF amplitude boosting.

The mask-programmed microprocessor J1 is the central control for the control unit. It is clocked by an 11.059 MHz crystal.

The soldered jumpers B6, B7, B8 at J1/4, 5, 6 set the status of the control unit. A power on reset at J1/10 guarantees that the processor will function faultlessly even after a drop in the operating voltage.

The display data for the vacuum fluorescent display H1 is read into the display drivers via the port lines P0.1...P0.7 and P3.6 of J1 and the 8-bit parallel-to-serial shift register J3.

With its frequency, PLL AF oscillator J2 synchronises data acceptance of the display drivers J7 and J8.

Via the data lines P3.0 and P3.1 (RxD, TxD), the control unit's processor communicates with the control processor on the control board (0850.410)

3.9.4 Converter Board

See circuit diagram: converter BG3 0831.910.310.203

The converter board supplies the necessary operating voltages for the display board.

A voltage of +5 V for the logical ICs is generated from +9 V by means of the voltage stabilizer J1.

To provide a display, the vacuum fluorescent display on the display board requires a +60 V anode voltage. To be able to separate electrons from the grid (cathode), an AC heating voltage (FF) also has to be applied. A half sinusoidal voltage is tapped from the output at D4 and is forwarded to the comparitor J2/1 via the voltage divider R17 and R8. J2/1 switches its output to high or low potential and charges or discharges C7. The changing level causes J3 to trigger the negative feedback stage V3, V8.

V5 as a switching transistor for the transformer T1 operates in the cycle of the switching frequency. C13 and R16, as well as C9, protect the circuit against retroactive effects of the transformer T1. J2/II monitors the 9 V line and prevents triggering of the display in the event of voltage errors. The 9 V operating potential in the SE unit is smoothed with the T network L1, L2 and C4.

3.9.5 Coding Board 2 kBytes

See circuit diagram: coding board 2 kBytes 0831.940.410.001

The coding board is located in the coding plug. It is equipped with the EEPROM J1. The data for operator-specific identification and the channels enabled for the data are stored here. They are read out by the processor on the display board of the control unit. This identifier can be read into the coding plug using a corresponding EEPROM programmer.

The coding plug is plugged into the right of the control unit by way of the microphone plug.

3.10 Interconnector SE 550

See circuit diagram 0831.170.410.002

The interconnector SE 550 is connected to the 15-pole connector X101 located on the rear side of the transceiver SE 550. It provides the following external interconnections:

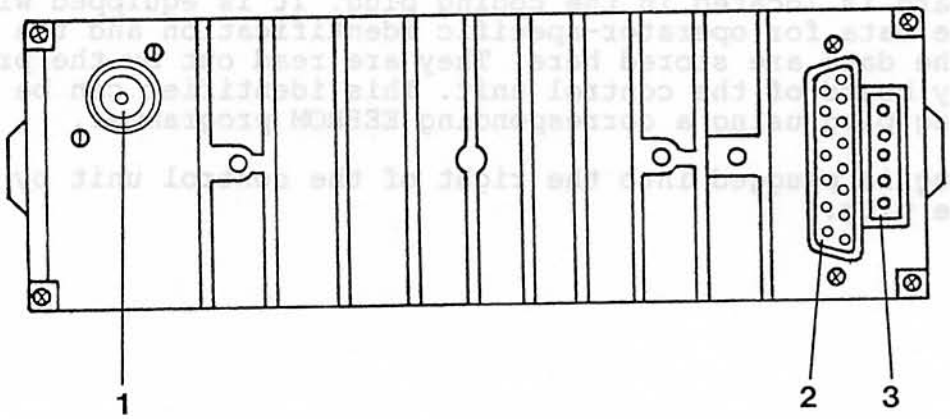
- battery voltage supply +UB 12 V (X4, X5)
- loudspeaker 4 Ω (B3)
- emergency keying by external PTT, active = low (B2/4)
- external signalization, max. 12 V/ 500 mA (B2/2)
- voltage output +UB 12 V (B2/3)

The line from B1/5 to B2/1 is a spare line. The diode D1 protects for confusing the poles.

3.11 External Interfaces (Pin-Assignment of Connectors)

The transceiver SE 550 provides the following connectors for external interconnections, given in sections 3.11.1, 3.11.2.

3.11.1 Transceiver Rear Side



1 X102 Connector BNC, 50 Ω
Antenna connector

2 X101 Connector 15-pole, D-Sub,
Main connector to interconnector SE 550 0831.170...

3 X103 Multipoint connector 5-pole
Cloning connector

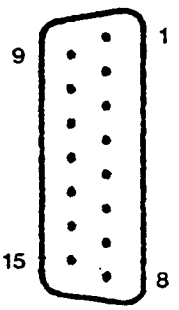
X102 BNC connector

BNC connector B2 located on antenna low pass 0831.300...
Impedance 50 Ω

X101 Connector 15-pole, D-Sub

Filter connector B1, 15-pole, D-Sub, located on interconnection board 0831.110...

X 101

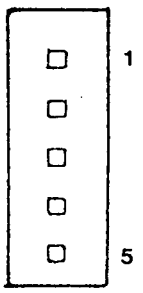


Pin	Designation	Explanation
1	+UB	+UB] Battery voltage
2	+UB	+UB] protected by external fuse
3	LSP ⊥	Loudspeaker 4 Ω
4	AS	Signalization, max. 12 V, 500 mA (BC817)
5	Res	Spare
6	AF Ear	AF earphone (600 Ω)
7	Gnd	Ground
8	Gnd	Ground
9	RF -10dB	RF power reduction -10 dB
10	LSP~	Loudspeaker
11	PTT A	Tx key PTTA, active = low
12	AFIN	AF 600 mV
13	Not	Emergency keying, active = low
14	+9V	+9 V •→
15	Mic A~	Microphone 100 mV

X103 Multipoint connector 5pole

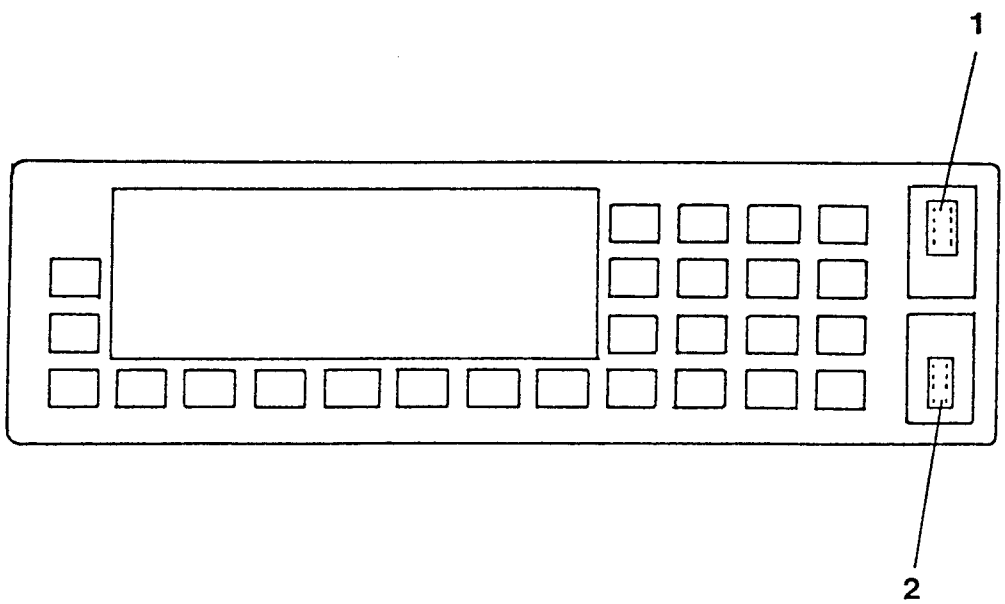
Multipoint connector B2, 5pole, located on interconnection board 0831.110...

X 103



Pin	Explanation
1	Cloning on
2	TxD
3	RxD
4	RTS
5	CTS

3.11.2 Control Unit, Front Side



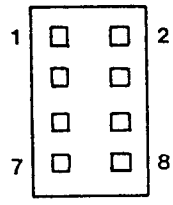
1 X104 Multipoint connector 8-pole
Coding plug connector 0831.000.000.941

2 X105 Multipoint connector 8-pole
Microphone or handset connector

X104 Multipoint connector 8-pole

Multipoint connector B4, 8-pole, located on display board 0831.920...

X 104

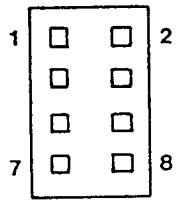


Pin	Designation	Explanation
1	DI	Data in
2	5V	5 V operating voltage
3	EN	Enable
4	DO	Data out
5	CL	Clock
6	⊥	Ground
7	-]	ON/OFF
8	-]	

X105 Multipoint connector 8-pole

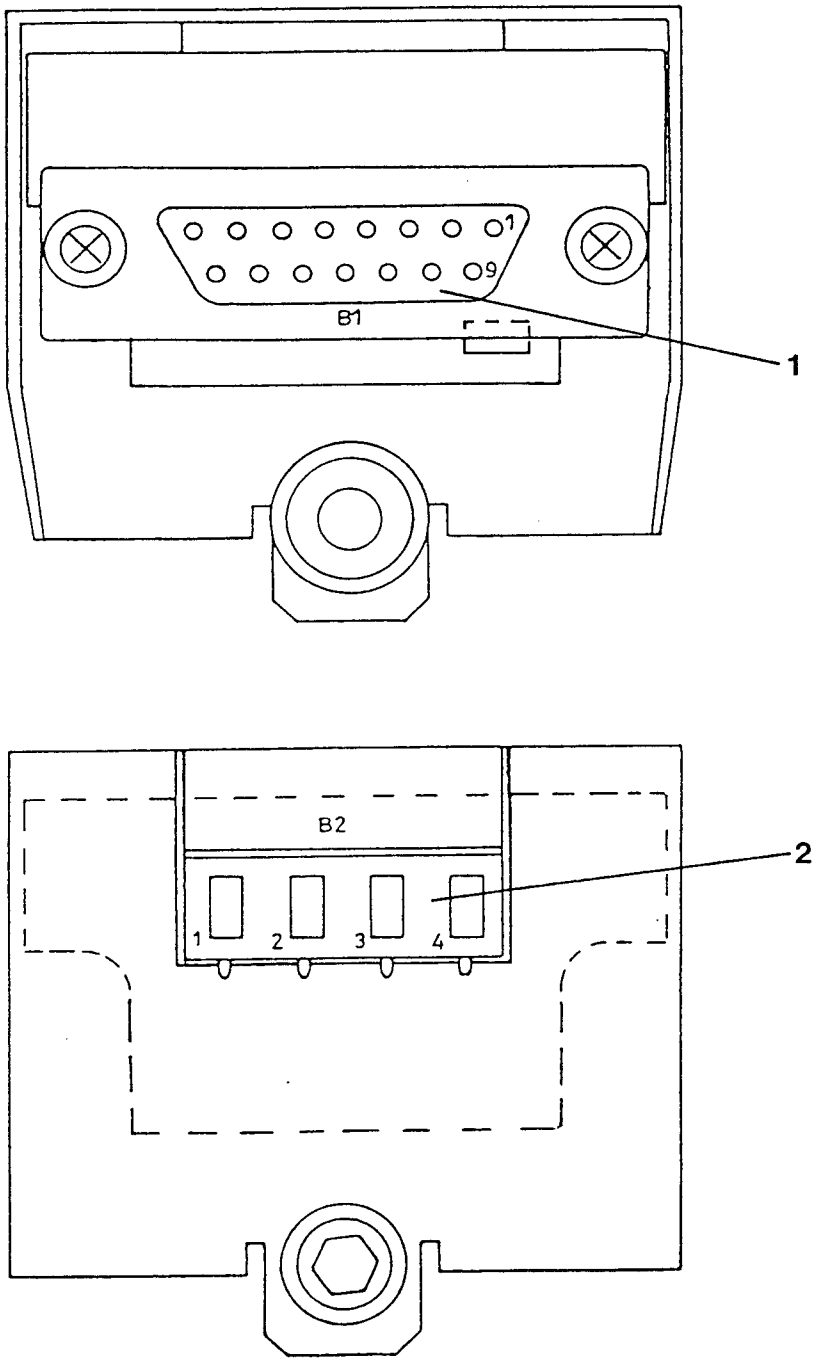
Multipoint connector B5, 8-pole, located on display board 0831.920...

X 105



Pin	Designation	Explanation
1	Mic B~	Microphone signal, 1 mV
2	HA	Cradle contact, not used
3	+9V	Microphone supply input, not used
4	PTT B	Tx keying PTTB, active = low
5	Ec~	Earphone
6	Mic ⊥	Ground microphone
7	Gnd	General ground
8	Ec ⊥	Ground earphone

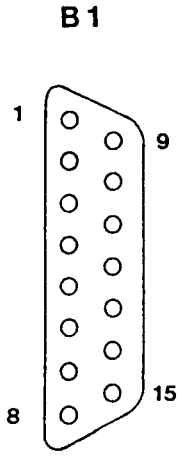
3.11.3 Interconnector SE 550



1 B1 Connector 15-pole, D-Sub
Transceiver connector

2 B2 Terminal strip 4-pole (X111)
Signalization, +UB, emergency keying

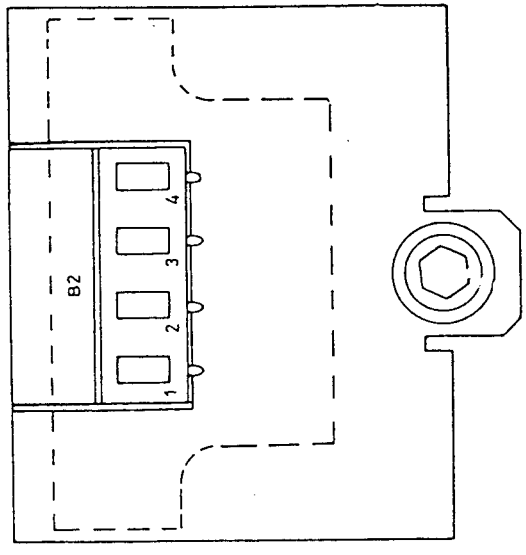
B1 Connector 15-pole, D-Sub



Pin	Designation	Explanation
1	+UB	+UB] Battery voltage
2	+UB	+UB] protected by external fuse
3	LSP ⊥	Loudspeaker 4 Ω
4	AS	Signalization, max. 12 V, 500 mA (BC817)
5	Res	Spare
6	AF Ear	AF earphone (600 Ω)
7	Gnd	Ground
8	Gnd	Ground
9	RF -10dB	RF power reduction -10 dB
10	LSP~	Loudspeaker
11	PTT A	Tx key PTTA, active = low
12	AFIN	AF 600 mV
13	Not	Emergency keying, active = low
14	+9V	+9 V •→
15	Mic A~	Microphone 100 mV

X111 Terminal strip 4-pole (B2)

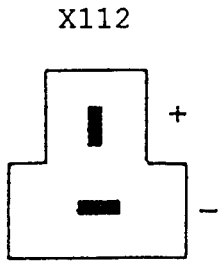
X 111



Pin	Designation	Explanation
1	Res	Spare line
2	AS	Signalization, max. 12 V, 500 mA
3	+UB	Battery voltage
4	Not	Emergency keying, active = Low

X112 Flat connector 2-pole (X5)

Battery voltage supply connector +UB, +UB protected by external fuse



Pin	Explanation
+	+UB Battery voltage, protected by external fuse
-	Ground

X113 Clamp 2-pole (B3)

Connection to loudspeaker